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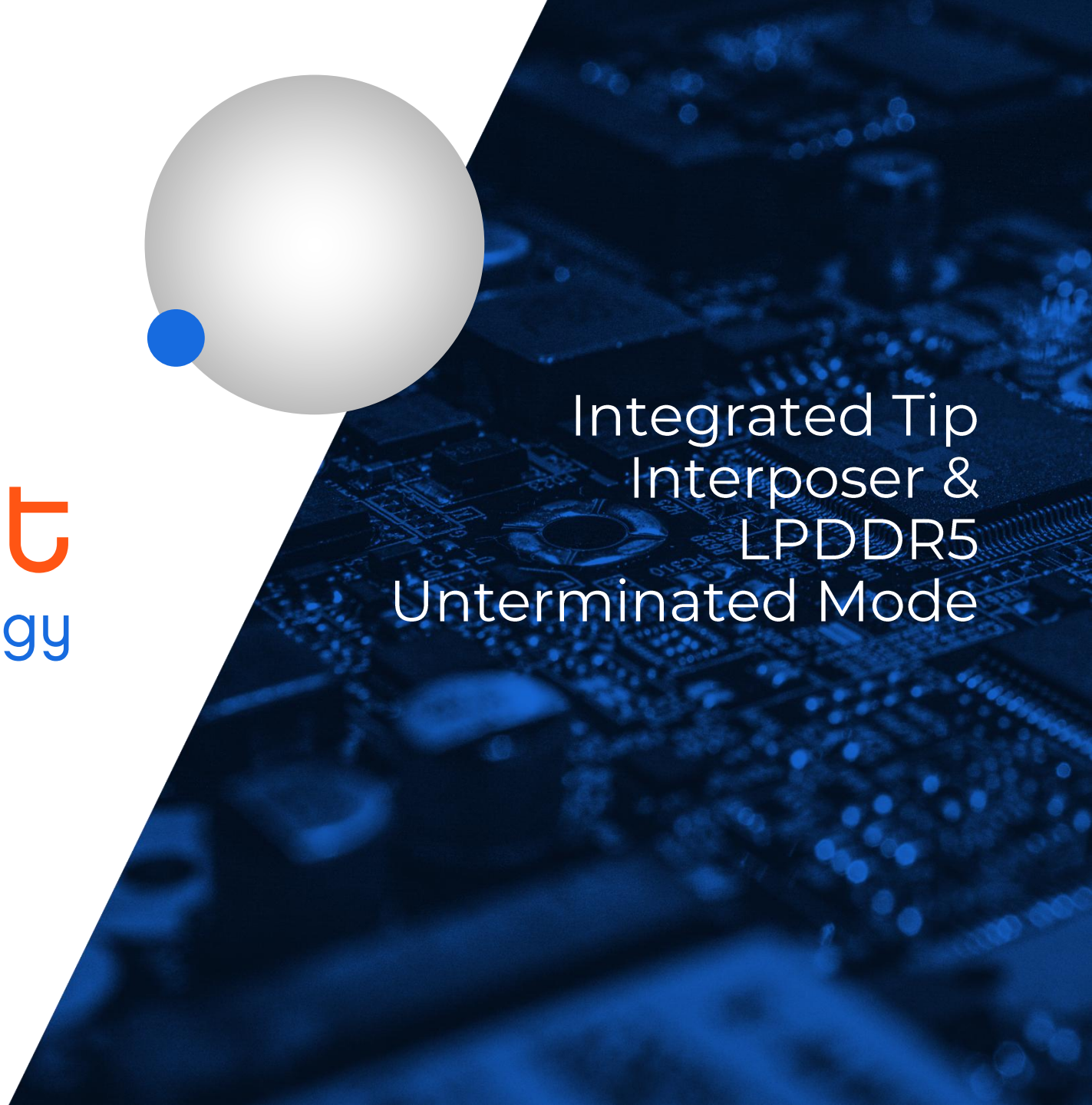
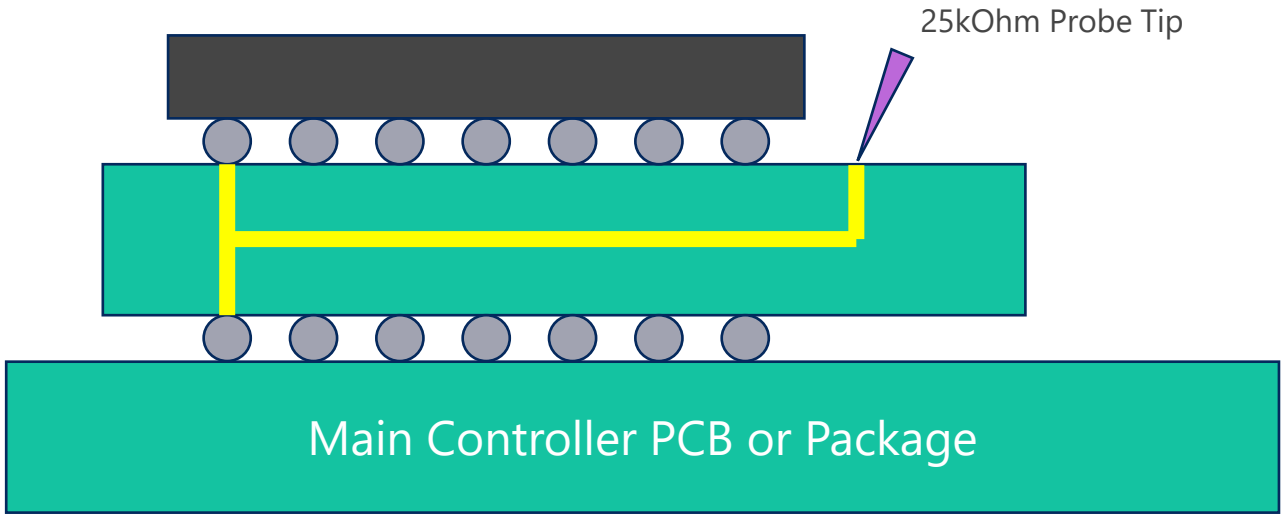
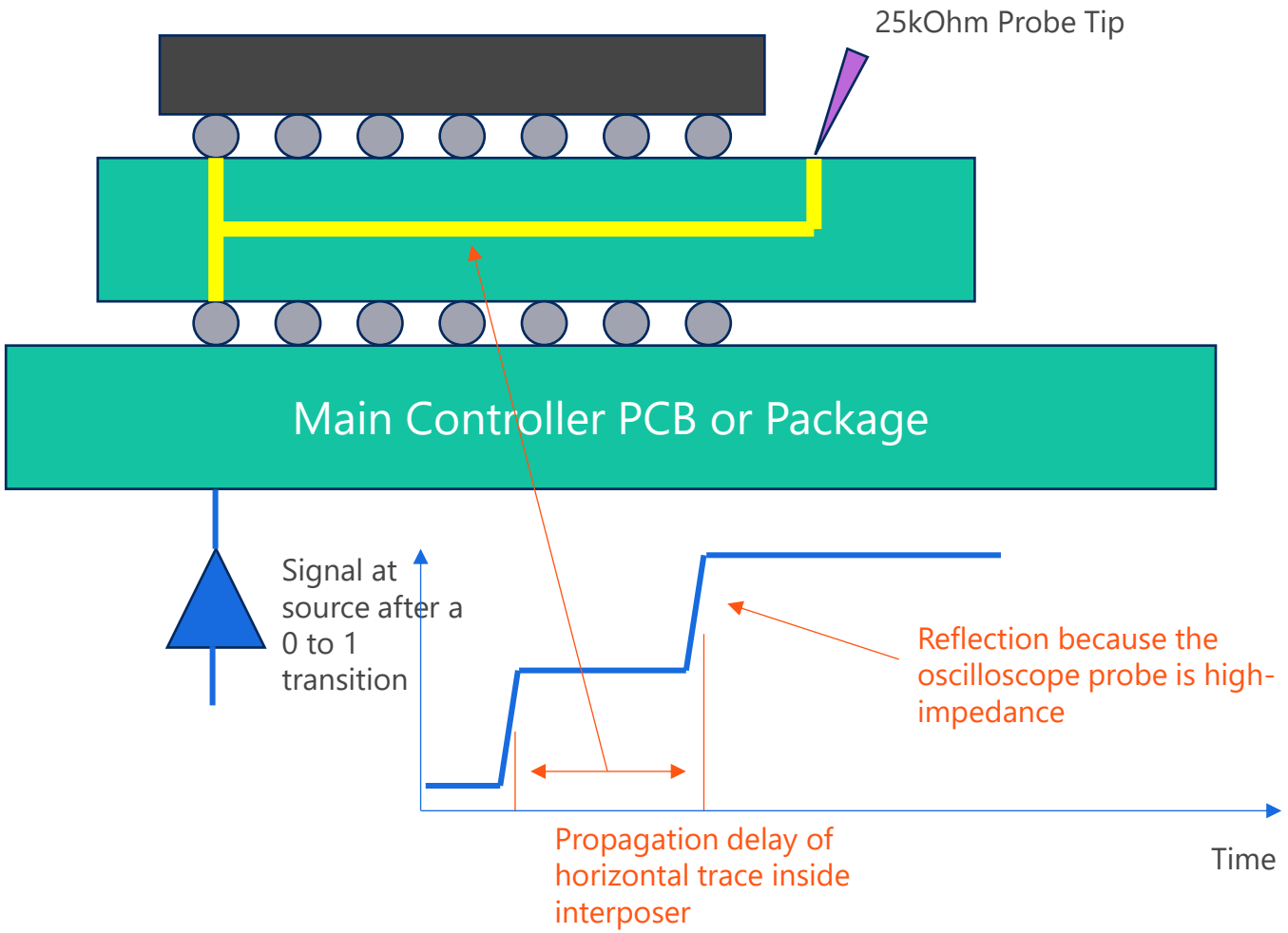
Integrated Tip Interposer & LPDDR5 Unterminated Mode



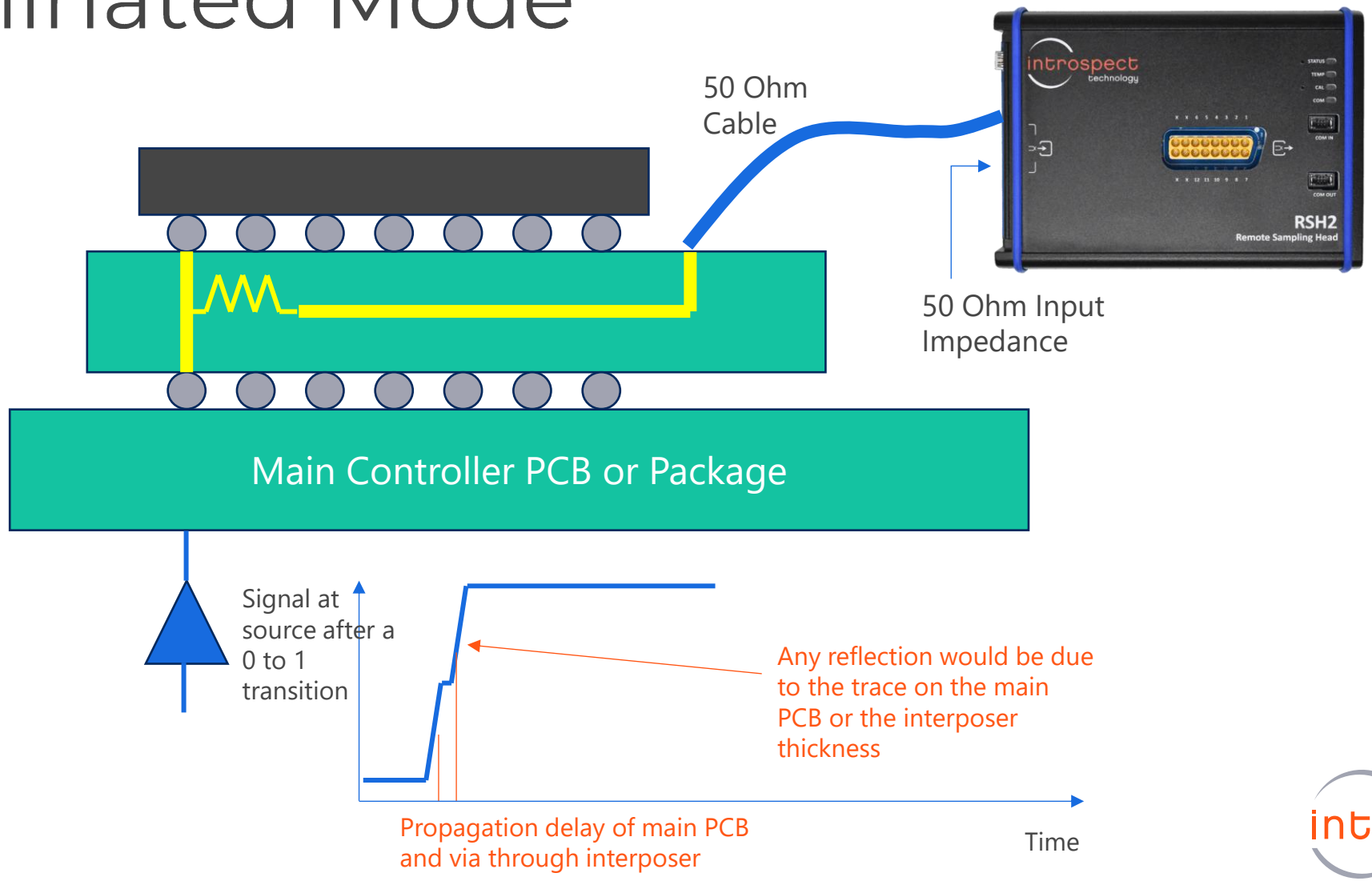
Normal Interposer



Normal Interposer in Unterminated Mode



Integrated Tip Interposer in Unterminated Mode



Return Loss Impact

T11 (TIME DOMAIN)

S11 (FREQUENCY DOMAIN)

The -30 dB performance means that any reflection seen in the signal will not be due to the interposer

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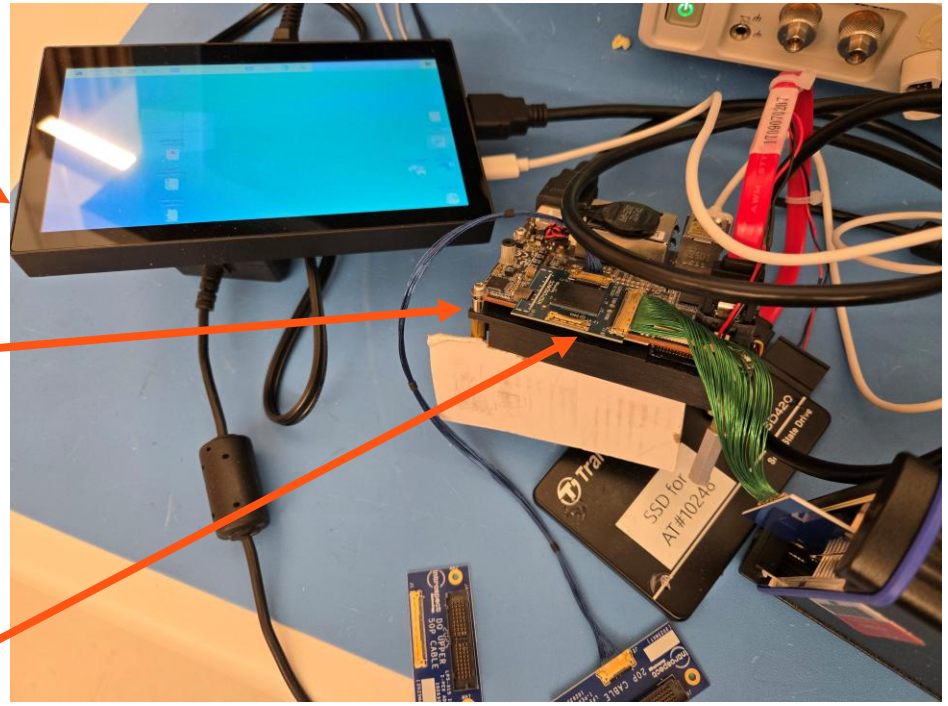
Real Example

Tiny PC display showing Microsoft Windows operation

Tiny PC with LPDDR5 315b package on the PCB away from the CPU (not Package on Package setup)



RSH2

Integrated-tip interposer with I-PEX connectors (Rev 0)

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WCK to RDQS Triggering (5.2 Gbps)

The red trace is WCK at 5.2 Gbps

The green trace is RDQS

We see good signal integrity and rise-time in terminated mode

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Unterminated CS at 1.3 Gbps CK Rate (5.2 Gbps WCK Rate)

On this Intel platform, the CK and CA bus is always unterminated even though the DQ runs at 5.2 Gbps.

Many customers told us that regular interposers do not work for unterminated LPDDR5 CK and CA bus.

But here, you can see that the integrated-tip interposer works very well!

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Unterminated CA at 1.3 Gbps (Explicit Clock on CK)

This is a CA signal (which toggles on both the rising edge and falling edge of the clock). This is why there is a duty cycle error with two transition bands. See next slide

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Unterminated CA at 1.3 Gbps (Explicit Clock on CK, Isolate Duty Cycle Error)

Here, we isolate the clock to show the duty cycle error on the same signal as the last page.

Again, the integrated-tip interposer works very well!

Very small reflection

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Terminated Mode Is Always Good…

- Next slides, show examples of the interposer on 8533 Mbps LPDDR5x 496b PoP device

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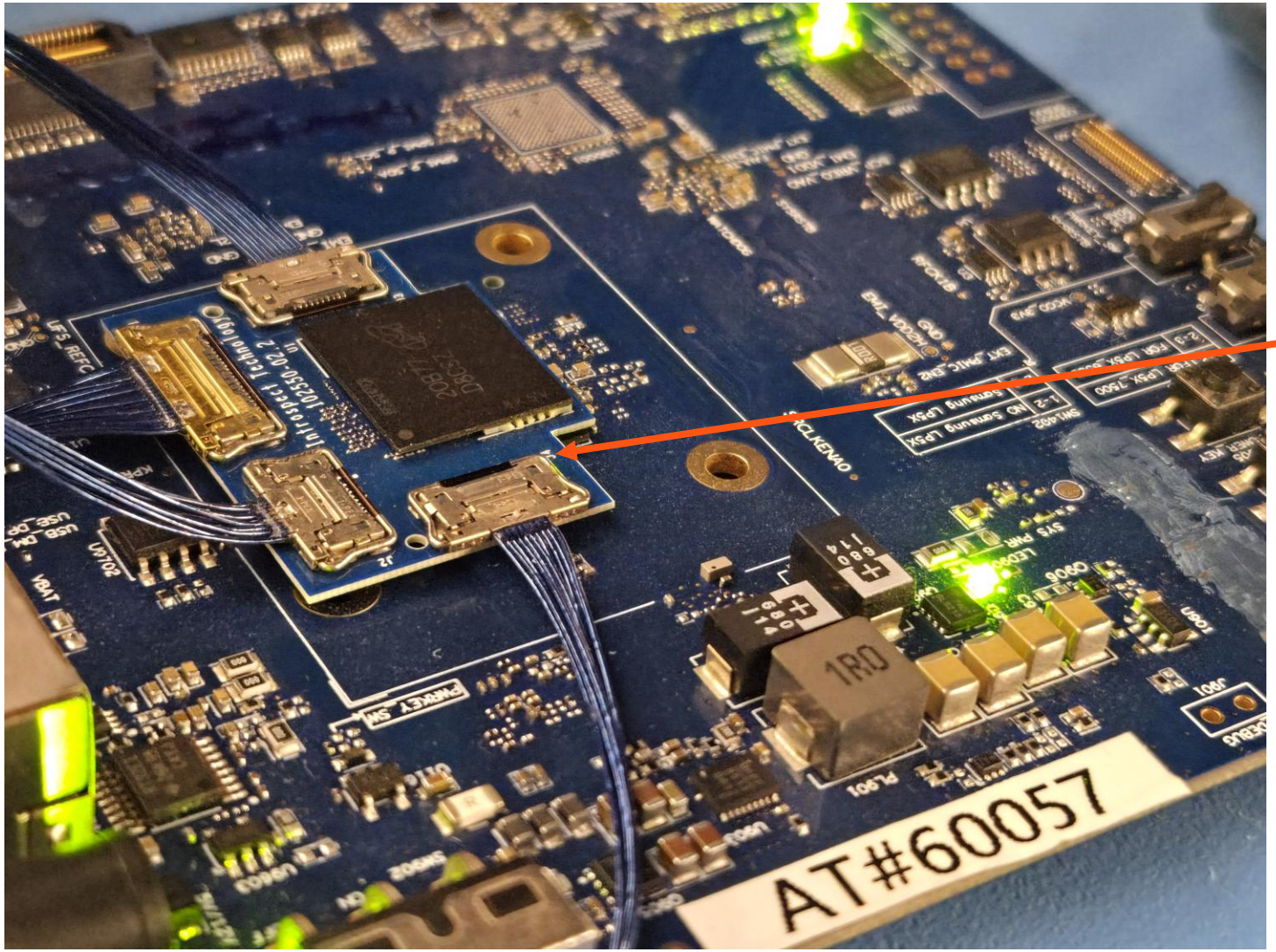
496b Package on Package LPDDR5x



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Interposer Performance

LIVE LPDDR5X FORMFACTOR PROBING AT 8533 MT/S

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Interposer Performance

LIVE LPDDR5X FORMFACTOR PROBING AT 8533 MT/S

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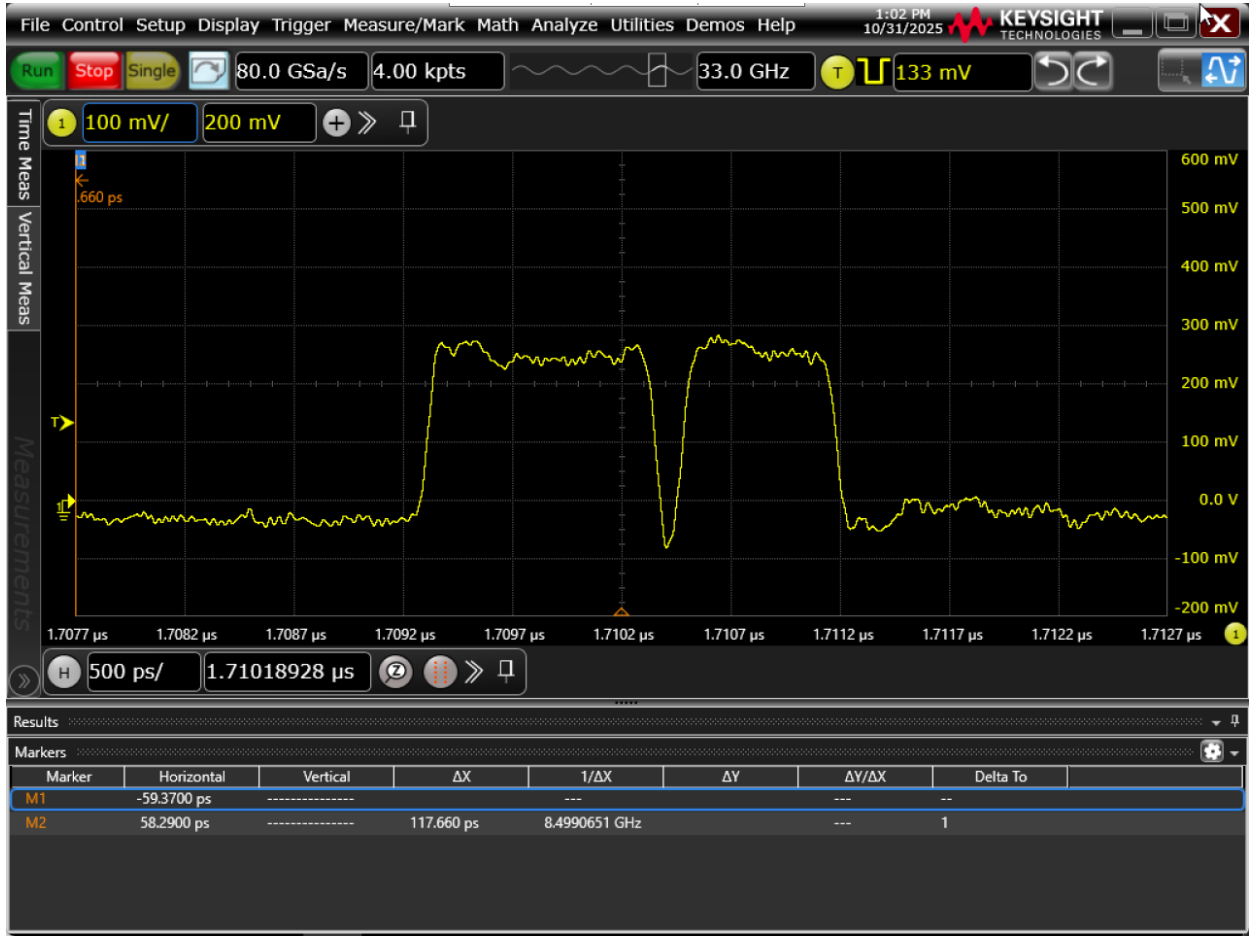
Interposer Performance

LIVE LPDDR5X FORMFACTOR PROBING AT 8533 MT/S



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